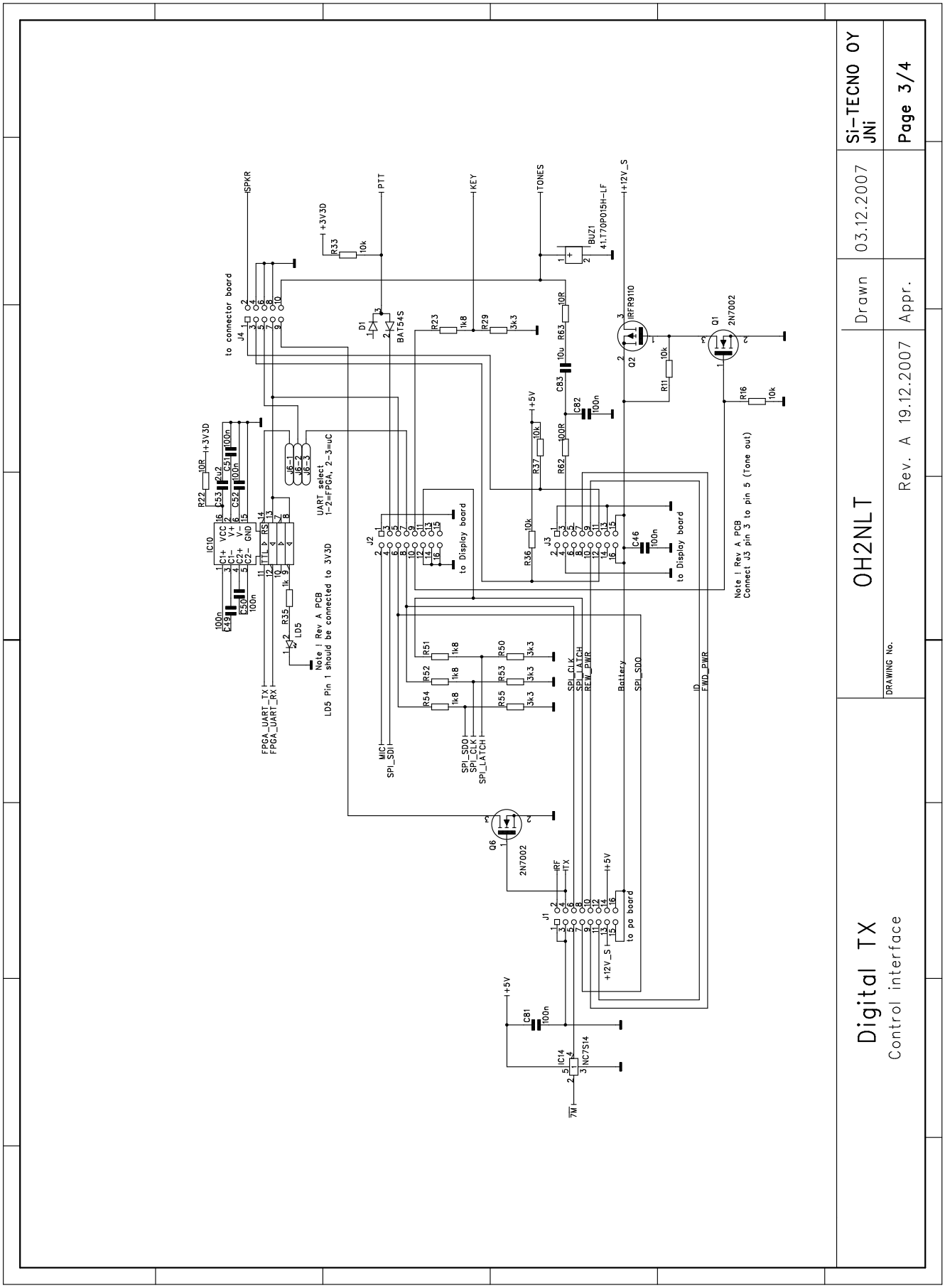
Digital TX
Control interface
OH2NLT
DRAWING No.
Drawn
Appr.
03.12.2007
Rev. A 19.12.2007
Si-TECNO OY
JNi
Page 3/4
to connector board
to Display board
to Display board
to pa board
UART select
1-2=FPGA, 2-3=uC
Note ! Rev A PCB
LD5 Pin 1 should be connected to 3V3D
Note ! Rev A PCB
Connect J3 pin 3 to pin 5 (Tone out)
SPKR
PTT
KEY
TONES
+3V3D
+5V
+12V_S
Battery
FWD_PWR
REV_PWR
SPI_CLK
SPI_LATCH
SPI_SDO
SPI_SDI
MIC
FPGA_UART_TX
FPGA_UART_RX
BUZ1
41.T70P015H-LF
D1
BAT54S
Q1
2N7002
Q2
IRFR9110
Q6
2N7002
IC10
IC14
NC7S14
J1
J2
J3
J4
J6-1
J6-2
J6-3
LD5
R22
R23
R29
R33
R35
R36
R37
R50
R51
R52
R53
R54
R55
R62
R63
R11
R16
C46
C50
C51
C52
C53
C81
C82
C83